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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
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ART UNIT	PAPER NUMBER
2615	

DATE MAILED: 12/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-13 and 15-30_ is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-13 and 15-30_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a)☐ All b)☐ Some * c)☐ None of:
   1.☐ Certified copies of the priority documents have been received.
   2.☐ Certified copies of the priority documents have been received in Application No. _____ .
   3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
      application from the International Bureau (PCT Rule 17.2(a)).
   * See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application)
   since a specific reference was included in the first sentence of the specification or in an Application Data Sheet.
   37 CFR 1.78.
   a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific
   reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)   4)☐ Interview Summary (PTO-413) Paper No(s). _____ .
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)   5)☐ Notice of Informal Patent Application (PTO-152)
3)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .   6)☐ Other: _____ .

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 22 September 2003 have been fully considered but they are

not persuasive.

Applicant argues:

1. Kameyama fails to teach or suggest the determination of **the number** of defective

    elements by analyzing the data during frame readout;

2. Vincent fails to teach or suggest the determination of the number of defective

    elements by analyzing the data **during frame readout**;

3. Heller fails to teach or suggest the determination of **the number** of defective

    elements by analyzing the data during frame readout;

4. The 103 for claim 15, based on Kameyama and Vincent, must be a typographical

    error since Claim 14 was rejected individually by both Kameyama and Vincent.

Examiners Answer:

1. Kameyama teaches the determination of the number of defective elements by

    analyzing the data during the frame readout. Such an arrangement is seen in that

    the number of defective pixels would be available after the complete frame was

    readout and analyzed by determining the index of the last space in memory used.

    Furthermore, be it a pointer system or indexed array, the amount of memory used

    for a fixed length address, and additional information, would indicate the number

    of address's stored, and thus the number of defective pixels.

2. Vincent inherently discloses the determination of the number of defective pixel elements by analyzing the data during frame readout in that the pixel information must be analyzed to appropriately distinguish the defective pixels, as stored in the external memory, so as to provide a correction or cover up function by the defect correction block during normal frame readout. Such an instance is implied in Column 2 lines 54 – 56, noting that the identification of the location of defective pixels (Such identification and storage is commonly known in the art as in Kameyama and Heller).

3. See examiners notes for argument 1 above.

4. The rejection for Claim 15 was not a typographical error as indicated by the applicant. Vincent was not used on it's own merits to reject Claim 15. Furthermore, it is seen that the reference (either Vincent or Kameyama) can be interpreted in multiple ways and that this rejection was based on an interpretation, such as that made by the client, that the art of record would not be seen to include all claimed limitations. This is not admittance that the art does not hold all claimed features, but merely another way of interpreting the art of record. Furthermore, it is seen that this rejection could have been made to reject all independent claims (1, 15 and 22) and the previous rejections of dependent claims under 102 (2 – 12, 15 – 17 and 21 – 28) could have been used as the teachings of similar rejections under 103.

It is noted that applicant, by the lack of request for an example of the office notice in

Claim 13, has admitted such features as prior art.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 – 6, 12, 15 – 17, 21 – 23, 27 and 28 are rejected under 35 U.S.C. 102(b) as

being anticipated by Kameyama et al. (U.S. Patent 5, 416, 516).

Regarding Claim 1, Kameyama disclose the method of detecting defective elements

comprising the steps of:

- Reading out a frame of sensing element data from an array (Column 4 lines 64 –

  66);

- Determining the number of defective elements by analyzing said data during the

  frame read out (Column 2 lines 3 – 16, Column 6 lines 4 – 25, Column 7 lines 7 –

  16, Column 10 line 60 – Column 11 line 20, Column 20 lines 37 – 58, Column 21

  lines 53 – 57).

Regarding Claim 2, Kameyama discloses:

- Imaging array (Figure 3 item 2);

- Programmably setting high and low limits for said pixel intensity values (Column 6 lines 4 - 10).

Regarding Claim 3, Kameyama discloses:

- Programmably setting the high and low limits based on illumination conditions (Figure 5, Column 7 lines 7 – 16).

Regarding Claim 4, Kameyama discloses:

- Comparing the pixel intensity values measured by said array to the high and low limits (Column 10 line 60 – Column 11 line 20).

Regarding Claim 5, Kameyama discloses:

- Indicating a defect when a pixel's intensity value is higher than said high limit or lower than said low limit (Column 2 lines 3 – 16, Column 6 lines 4 – 25, Column 7 lines 7 – 16, Column 10 line 60 – Column 11 line 20, Column 20 lines 37 – 58, Column 21 lines 53 – 57).

Regarding Claim 6, Kameyama discloses:

- Imaging array (Figure 3 item 2);

- Identifying in the focal plane of the pixel array which pixel's are defective (Column 2 lines 3 – 16, Column 6 lines 4 – 25, Column 7 lines 7 – 16, Column 10 line 60 – Column 11 line 20, Column 20 lines 37 – 58, Column 21 lines 53 – 57, it is noted that all pixels are located on the focal plane).

Regarding Claim 12, Kameyama discloses:

- Storing information about the location of the defective elements in a memory in said array (Column 6 lines 4 – 25).

Regarding Claim 15, Kameyama discloses the medium that stores instructions that cause a processor-based system to:

- Programmably **set high and low limits** for pixel intensity values (Column 6 lines 4 - 10);

- **Determine** during a read out of pixel intensity values from the array, **the number of defective pixels** from said imaging array in view of said high and low limits for pixel intensity values (Column 2 lines 3 – 16, Column 6 lines 4 – 25, Column 7 lines 7 – 16, Column 10 line 60 – Column 11 line 20, Column 20 lines 37 – 58, Column 21 lines 53 – 57).

Regarding Claim 16, Kameyama discloses:

- Programmably set high and low limits based on illumination conditions (Figure 5, Column 7 lines 7 – 16).

Regarding Claim 17, Kameyama discloses:

- Comparing the pixel intensity values to the high and low limits (Column 10 line

   60 – Column 11 line 20).

Regarding Claim 21, Kameyama discloses:

- Storing information in a memory about the location of a defective pixel (Column

   6 lines 4 – 25).

Regarding Claim 22, Kameyama discloses:

- A plurality of sensing elements (Figure 3 item 2);

- Circuit adapted to determine the number of defective elements by analyzing the

   element data as it is read out from said elements (Column 2 lines 3 – 16, Column

   6 lines 4 – 25, Column 7 lines 7 – 16, Column 10 line 60 – Column 11 line 20,

   Column 20 lines 37 – 58, Column 21 lines 53 – 57).

Regarding Claim 23, Kameyama discloses:

- Device is an imaging device (Figure 3 item 2);

- Elements are pixels (Figures 1a, 1b, 2a, 2b);

- Storage adapted to enable high and low limits for pixel intensity values to be set

   programmably (Figure 5, Column 7 lines 7 – 16, Column 10 line 60 – Column 11

   line 20, Figure 26 items 117 and 118).

Regarding Claim 27, Kameyama discloses:

- Memory adapted to store information about the location of defective elements

  (Column 6 lines 4 – 25).

Regarding Claim 28, Kameyama discloses:

- Memory includes a location corresponding to each of a plurality of elements

  (Column 6 lines 4 – 25, Column 11 lines 30 – 44);

Claims 1, 7 – 11, 22 and 24 – 26 are rejected under 35 U.S.C. 102(b) as being anticipated

by Vincent (U.S. Patent 5, 436, 659).

Regarding Claim 1, Vincent disclose the method of detecting defective elements

comprising the steps of:

- Reading out a frame of sensing element data from an array (inherent);

- Determining the number of defective elements by analyzing said data during the

  frame read out (Column 8 line 24 – Column 12 line 24).

Regarding Claim 7, Vincent discloses:

- Imaging array (Figure 1 item 16);

- Data is pixel data (Column 2 lines 54 – 56);

- Determining the number of spatial defects by analyzing said pixel data (Column

  11 line 61 – Column 12 line 24).

Regarding Claim 8, Vincent discloses:

- Determining whether two defective pixels are closer together than a

  programmable offset (Column 9 lines 26 – 31).

Regarding Claim 9, Vincent discloses:

- Adding a column or row address where a defective exists to a programmable

  offset and storing said address with said offset (Column 8 line 24 – Column 11

  line 9).

Regarding Claim 10, Vincent discloses:

- Comparing the address of a defective pixel to a stored address plus a

  programmable offset (Column 8 lines 42 – 58).

Regarding Claim 11, Vincent discloses:

- Identifying the number of spatial defects by column and row by analyzing said

  data (Column 10 line 56 – Column 11 line 2).

Regarding Claim 22, Vincent discloses:

- A plurality of sensing elements (Figure 1 item 16);

- Circuit adapted to determine the number of defective elements by analyzing the element data as it is read out from said elements (Column 8 line 24 – Column 12 line 24).

Regarding Claim 24, Vincent discloses:

- Determining the number of spatial defects by analyzing said pixel data (Column 11 line 61 – Column 12 line 24).

Regarding Claim 25, Vincent discloses:

- Window circuit adapted to add a column or row address where a defective exists to a programmable offset and storing said address with said offset (Column 8 lines 42 – 58).

Regarding Claim 26, see examiners comments for Claim 10.

Claims 22, 29 and 30 rejected under 35 U.S.C. 102(e) as being anticipated by Heller et al. (U.S. Patent 6, 293, 465 B1).

Regarding Claim 22, Heller discloses:

- A plurality of sensing elements (Figure 2 item 12);

- Circuit adapted to determine the number of defective elements by analyzing the element data as it is read out from said elements (Column 7 line 58 – Column 8 line 41).

Regarding Claim 29, Heller discloses:

- Circuit and elements are formed on the same die (Column 3 line 54 – Column 4

    line 9, Column 8 lines 17 – 20, it is noted that this is formed on a single chip).

Regarding Claim 30, Heller discloses:

- Imaging device (Figure 2 item 12);

- Pixels (Figure 2 item 12);

- Circuit being formed on the imaging device's focal plane that includes said pixels

    (Figure 2, single chip unit wherein the pixel array is formed on the focal plane and

    the control circuit is formed next to the array).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kameyama et al.

(U.S. Patent 5, 416, 516).

Regarding Claims 13, Kameyama fails to specifically discloses:

- Each element in the array has a corresponding location in the memory and setting a defect exists bit at each memory location where a defective element has been identified;

OFFICIAL NOTICE:

It is well known to include a location in memory for every pixel and to indicate that the pixel is defective with setting of a bit. Such an arrangement would have been advantageous in providing a system in which a known memory size is used for each image sensor and the system used would benefit from an increase in speed in that the system would only have to process a single bit to know if there is a defect at the location of interest.

Therefore, it would have been obvious to one of ordinary skill in the art to include the location in memory for every pixel and to indicate that the pixel is defective with setting of a bit and to use an external tester to implement the read sequencing of the memory speed up the system by having the processor process a single bit to know if there is a defect at the location of interest.

Claims 15 and 18 - 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vincent (U.S. Patent 5, 436, 659) in view of Kameyama et al. (U.S. Patent 5, 416, 516).

Regarding Claim 15, Vincent discloses the medium that stores instructions that cause a processor-based system to:

- Provide the system for testability, including counting, wherein the system is provided for improving a method of dealing with defective pixels (Column 8 line 24 – Column 12 line 24).

Vincent does not specifically disclose the method of determining which pixels are defective, specifically:

- Programmably **set high and low limits** for pixel intensity values;

- **Determine** during a read out of pixel intensity values from the array, **the number of defective pixels** from said imaging array in view of said high and low limits for pixel intensity values.

Kameyama teaches:

- Programmably **set high and low limits** for pixel intensity values (Column 6 lines 4 - 10);

- **Determine** during a read out of pixel intensity values from the array, **the number of defective pixels** from said imaging array in view of said high and low limits for pixel intensity values (Column 2 lines 3 – 16, Column 6 lines 4 – 25, Column 7 lines 7 – 16, Column 10 line 60 – Column 11 line 20, Column 20 lines 37 – 58, Column 21 lines 53 – 57).

Such a method is a well known in the art for determining a defective pixel and would be useful in obtaining information as to which pixels are flawed.

Therefore, it would have been obvious to one of ordinary skill in the art to include the medium that stores instructions that cause a processor based system to programmably set high and low limits for pixel intensity values and Determine during a read out of pixel intensity values from the array, the number of defective pixels from said imaging array in view of said high and low limits for pixel intensity values so as to determine which pixels are defective.

Regarding Claim 18, Vincent discloses:

- Determining the number of spatial defects by analyzing said pixel data (Column 11 line 61 – Column 12 line 24).

Regarding Claim 19, Vincent discloses:

- Determining whether two defective pixels are closer together than a programmable offset (Column 9 lines 26 – 31).

Regarding Claim 20, Vincent discloses:

- Identifying the number of spatial defects by column and row by analyzing said data (Column 10 line 56 – Column 11 line 2).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing

date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Eric D Wisdahl whose telephone number is (703) 305-4915. The

examiner can normally be reached on 9:00 - 6:00 Mon-Thur every other Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Andrew Christensen can be reached on (703) 308-9644. The fax phone number for

the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the technology center 2600 customer service office which can be reached at

telephone number (703) 306-0377.

edw

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